(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 032 033 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
30.08.2000 Bulletin 2000/35

(51) Int. Cl.[7]: **H01L 21/8234**, H01L 21/28, H01L 21/8238

(21) Application number: **00103406.5**

(22) Date of filing: **24.02.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **26.02.1999 US 121786 P**

(71) Applicant:
Texas Instruments Incorporated
Dallas, Texas 75251 (US)

(72) Inventors:
- **Wilks, Glen D.**
  Dallas, Texas 75243 (US)
- **Summerfelt, Scott R.**
  Cupertino, California 95014 (US)

(74) Representative:
Schwepfinger, Karl-Heinz, Dipl.-Ing.
Prinz & Partner GbR
Manzingerweg 7
81241 München (DE)

(54) Method of forming dual metal gate structures for CMOS devices

(57) An embodiment of the instant invention is a method of forming a first transistor having a first gate electrode and a second transistor having a second gate electrode on a semiconductor substrate, the method comprising the steps of: forming a conductive material (step 216 of FIGURE 2) insulatively disposed over the semiconductor substrate, the conductive material having a work function; and altering a portion of the conductive material (step 218 of FIGURE 2) so as to change the work function of the altered conductive material, the conductive material to form the first gate electrode and the altered conductive material to form the second gate electrode. Preferably, the first transistor is an NMOS device, the second transistor is a PMOS device, and the first transistor and the second transistor form a CMOS device. The conductive material is, preferably, comprised of a conductor selected from the group consisting of: Ta, Mo, Ti and any combination thereof. Preferably, the step of altering a portion of the conductive material is comprised of: subjecting the portion of the conductive material to a plasma which incorporates a nitrogen-containing gas.

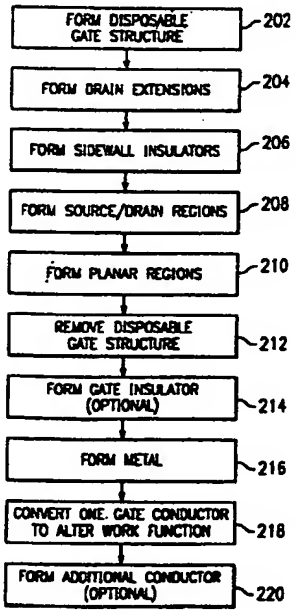

FIG. 2

EP 1 032 033 A2

Description

FIELD OF THE INVENTION

[0001] The instant invention pertains to semiconductor device fabrication and processing and more specifically to a method of fabricating a metal gate structures for CMOS devices.

BACKGROUND OF THE INVENTION

[0002] As electronic devices become more and more complex, the need for greater and greater numbers of transistors on the device is increased. In addition, power consumption needs to be reduced while the speed of the devices needs to be increased. At least part of the answer to these requirements involves reducing the area that each transistor occupies. However, this may adversely affect one or more of the other requirements. More specifically, as the transistors are scaled down, the gate structure is also scaled down and this increases the resistance of the gate. Hence, the power consumption is increased and the speed of the device is decreased.

[0003] Several attempts to reduce the sheet resistivity of the gate structures have been made in the past. First, the polycrystalline silicon was more heavily doped with either n-type or p-type dopants. Then, the upper portion of the gate was silicided with tungsten or titanium. Presently, cobalt suicide is being used so as to reduce the resistivity for smaller geometries. The next likely solution will involve metal gate structures.

[0004] Metal gate structures provide lower sheet resistivity virtually irrespective of the width of the gate. However, many metal gate materials have problems which must be overcome before they can be implemented in a standard semiconductor processing flow. One problem is that many metals are unstable next to SiO_2, which is commonly used for the gate dielectric layer. Another problem is that many metals become less conductive when they are oxidized.

[0005] Aluminum and tungsten have been used to form gate structures. Aluminum may not be a good choice due to the problems stated above and tungsten has a work function which lies between the work function of p-type polycrystalline silicon (poly) and n-type poly. A problem with tungsten, though, is that as the applied voltages become smaller and smaller the fact that the work function is midgap and is unchangeable (as compared to n-type and p-type poly), it may become difficult to provide a gate potential greater than the threshold voltage of the PMOS and NMOS device.

[0006] In an attempt to over come this threshold voltage problem using one midgap metal for both PMOS and NMOS device, aluminum has been utilized for one type of devices while platinum is used for the other type of devices. However, platinum is expensive and difficult to work with and aluminum suffers from the problems listed above. Hence, a need exists for a gate electrode material whose conductivity is not relative to the gate width and which has different work functions for PMOS devices and NMOS devices.

SUMMARY OF THE INVENTION

[0007] An embodiment of the instant invention is a method of forming a first transistor having a first gate electrode and a second transistor having a second gate electrode on a semiconductor substrate, the method comprising the steps of: forming a conductive material insulatively disposed over the semiconductor substrate, the conductive material having a work function; and altering a portion of the conductive material so as to change the work function of the altered conductive material, the conductive material to form the first gate electrode and the altered conductive material to form the second gate electrode. Preferably, the first transistor is an NMOS device, the second transistor is a PMOS device, and the first transistor and the second transistor form a CMOS device. The conductive material is, preferably, comprised of a conductor selected from the group consisting of: Ta, Mo, Ti and any combination thereof. Preferably, the step of altering a portion of the conductive material is comprised of: subjecting the portion of the conductive material to a plasma which incorporates a nitrogen-containing gas.

[0008] Another embodiment of the instant invention is a method of forming a first transistor having a first gate electrode and a second transistor having a second gate electrode on a semiconductor substrate, the method comprising the steps of: forming a first conductive material insulatively disposed over a first portion of the semiconductor substrate, the first conductive material having a first work function; forming a second conductive material insulatively disposed over a second portion of the semiconductor substrate, the second conductive material is comprised of the first conductive material but has a second work function which is different than the first work function; and wherein the first conductive material is used to form the first gate electrode and the second conductive material is used to form the second gate electrode. In one alternative embodiment, the first conductive material is comprised of Ta and the second conductive material is comprised of Ta_xN_y. In another alternative embodiment, the first conductive material is comprised of Mo and the second conductive material is comprised of Mo_xN_y. In yet another alternative embodiment, the first conductive material is comprised of Ti and the second conductive material is comprised of Ti_xN_y.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

FIGURE 1 is a cross-sectional diagram of a par-

tially fabricated CMOS device of the method of one embodiment of the instant invention.

FIGURE 2 is a flow diagram of a method of an embodiment of the instant invention.

FIGUREs 3a-3e are cross-sectional views of a partially-fabricated semiconductor device using the method of the instant invention as illustrated in FIGURE 2.

FIGURE 4 is a chart illustrating the work functions of different materials.

[0010] Like reference numerals or symbols in different figures refer to corresponding structures unless indicated otherwise. The figures are provided merely to illustrate the concepts of the instant invention. The figures are not drawn to scale.

DETAILED DESCRIPTION OF THE DRAWINGS

[0011] In essence, the instant invention involves a CMOS device and a method for making the device which incorporates a metal gate electrode for either the NMOS device or the PMOS device and an altered version of the metal for the gate electrode of the other device, PMOS device or NMOS device (respectively). Preferably, the instant invention involves forming the gate electrode of the NMOS device, at least in part, of tantalum and the gate electrode of the PMOS device, at least in part, of tantalum nitride. Hence, the instant invention involves the same base metal, for example, tantalum, but uses an altered form of the base metal for one of the devices gate electrode. The instant invention may be fabricated using a disposable gate methodology (basically illustrated in FIGUREs 2 and 3a-3e) or with the traditional gate formation methodology (basically illustrated in FIGURE 1).

[0012] Referring to FIGURE 1, the CMOS device 100 of the instant invention can be fabricated using traditional techniques or it may be fabricated using the disposable gate methodology illustrated in FIGUREs 2 and 3a-3e. The traditional methodology of forming gate structures involves forming isolation structures 118 which may be LOCOS type isolation structures, shallow trench isolation structures (STI - shown in FIGURE 1 as isolation structures 118), or doped isolation regions. A gate insulator layer 112, 120 is formed along with an overlying gate conductor layer 106, 108. In the instant invention, the gate insulating layer is preferably comprised of silicon dioxide, silicon nitride, a high dielectric constant material (such as PZT, BST, tantalum pentoxide, or other commonly used material), a silicate, a combination of one or more of the above, an oxynitride, or a stack thereof. The gate conductor layer is preferably comprised of a metal which can be selectively altered so as to change its work function. Examples of these are titanium, tantalum, molybdenum, or other similar metal. Either prior to the patterning and etching of the gate structure or after these steps, a portion of the gate conductor is converted so as to change its work function. Preferably, this is accomplished by either nitriding this portion of the conductive layer (or a portion of the already patterned and etched gate structures) or using a metal/nitride/metal stack on this portion of the gate structures so that annealing this layer of metal will distribute nitrogen throughout. Since the conductive material is relatively thin (preferably on the order of 5 to 50 nm), these portions to be nitrided can be nitrided by annealing this portion of the layer (or these particular gate conductors which are already patterned and etched) in a nitrogen-containing atmosphere (such as ammonia), or subjecting the selected portions of the conductive layer or gate structures to a nitrogen-containing gas (preferably N_2) which is incorporated into a plasma. However, instead of nitriding portions of an already formed conductive layer, the PMOS gate structure 108/120 can be formed separately from the NMOS gate structure 106/112. Hence, one gate structure can be formed of Ta, Mo or Ti and the other can be co-deposited with either Ta, Mo or Ti and a nitrogen-containing source (such as N_2). Alternatively, the nitrided version can be comprised of a stack of either Ta, Mo or Ti and a nitrogen-containing layer (such as TaN, MoN or TiN) and then annealed so as to distribute the nitrogen throughout these gate structures. Preferably, the gate conductor 106 of the NMOS device 102 will be comprised of Ta, Mo or Ti and the gate conductor 108 of PMOS device 104 will be comprised of nitrogen and either Ta, Mo, Ti, or a combination thereof.

[0013] After the gate structures are formed, source/drain extensions (if used) and the source/drain regions 114 and 116 are formed. Standard processing follows after this.

[0014] Another embodiment of the instant invention is illustrated in FIGUREs 2 and 3a-3e. The details of this embodiment are applicable to the above embodiment. Referring to step 202 of FIGURE 2 and FIGURE 3a, isolation structures 316 are formed. Isolation structures 316 may be comprised of LOCOS, STI, or doped isolation regions. First and second dummy layers are formed, next. The first dummy layer may be comprised of the material to form the gate insulator or it may simply be a dummy layer. If the first dummy layer is comprised of the gate insulating material (preferably silicon dioxide, silicon nitride, an oxynitride, BST, tantalum pentoxide, a silicate, or other suitable gate insulating material) then this layer will not be later removed and gate insulating layer 324 will not be formed in step 214. The first and second dummy layers are patterned and etched so as to form the dummy gate structures for PMOS device 302 and NMOS device 304. The dummy gate structure is comprised of two layers. If the bottom layer (layers 310 and 311) are not actually comprised of the gate insulating material, then it should be comprised of a material that can be removed without damaging the substrate 301 or adversely affect the surrounding structures when it is removed in step 212. If the first layer is

a removable layer, then the first and second layers may be comprised of the same material. Hence, structures 310 and 306 and 311 and 308 would be comprised of the same materials. Preferably, these structures are comprised of a material that, when removed, will not substantially adversely affect the underlying substrate 301 or the surrounding structures (such as sidewall insulators 318 and 319 and planar insulating material 322). Therefore, structures 310, 306, 311, and 308 may be comprised of silicon nitride, silicon dioxide, polycrystalline silicon, silicon germanium, or any other material that can be removed selective to the underlying silicon substrate and the oxide or nitride sidewall insulators.

[0015] Referring to step 204 of FIGURE 2, source/drain extensions are formed (if at all) using the isolation structures 316 and disposable gate structures (structures 310/306 and 311/308) to align to. The source/drain extensions 312 of PMOS device 302 are preferably comprised of a p-type dopant (such as boron) and the source/drain extensions 314 of NMOS device 304 are preferably comprised of n-type dopants (such as phosphorous or arsenic).

[0016] Referring to step 206 of FIGURE 2 and FIGURE 3b, sidewall insulators 318 and 319 are formed. Sidewall insulators 318 and 319 may be comprised of thermally grown silicon oxide, deposited silicon oxide, silicon nitride, an oxynitride, or a combination or stack thereof. Referring to step 208, source/drain regions 313 and 315 are formed, next. Preferably, source/drain regions 313 are formed by doping boron into the substrate, and source/drain regions 315 are formed by doping arsenic and/or phosphorous into the substrate.

[0017] Referring to step 210 of FIGURE 2 and FIGURE 3c, insulating layer 322 is formed. Preferably, insulating layer 322 is either flowed onto the wafer so as to have its top surface at roughly the same height as the top of the disposable gate structure and sidewall insulators. However, insulating layer 322 may be deposited or flowed onto the wafer and then polished down to be coextensive with the disposable gate structure and sidewall insulators using chemical-mechanical polishing (CMP). Preferably, insulating layer is comprised of a flowable oxide (such as aerogel, xerogel, or HSQ), BPSG, TEOS, PETEOS, PSG, FSG, or other silicon oxide material.

[0018] Referring to FIGURE 3d and step 212 of FIGURE 2, the disposable gate structures (structures 306 and 308 and structures 310 and 311 if they are not comprised of the gate insulating material) are removed. Preferably, this is accomplished so that neither the substrate 301, sidewall insulators 318 and 319, insulating layer 322 nor the gate insulators 310 and 311 (if they are formed of the gate insulating material which is desired for these devices) are substantially degraded or etched away.

[0019] Referring to step 214 of FIGURE 2, if structures 310 and 311 are not comprised of the desired gate material and are removed in step 212, gate insulating layer 324 is formed. Gate insulating material is preferably comprised of silicon dioxide, silicon nitride, an oxynitride, a silicate, or a high-k material (such as BST, tantalum pentoxide, or other suitable material).

[0020] Conductor 326 is formed in step 216 of FIGURE 2. Preferably, conductor 326 is comprised of Ta, Mo, Ti or other suitable conductor which can be selectively altered so as to selectively change its work function. However, a portion of conductor 326 may be comprised of Ta, Mo or Ti while the other portion is comprised of an altered form of Ta, Mo or Ti (preferably a nitrided version). The altered form can be one in which Ta, Mo or Ti is co-deposited with nitrogen or it can be a stack of Ta, Mo and/or Ti and a nitride. Preferably, conductor 326 is comprised of either Ta, Mo or Ti and is later altered. Conductor 326 should be thick enough so that its work function defines the functioning of the gate. Preferably, the thickness of conductor 326 is on the order of around 5 to 50 nm (roughly around 8 to 10 unit cells or more in thickness)

[0021] Either prior to the patterning and etching of conductor 326 and insulating layer 324 or after this step, one portion (or one of the gate conductors - conductor 327) is altered so as to change its work function (step 218). This can be accomplished by masking off the portion of conductor 326 (or conductor 327) and subjecting the exposed portion of conductor 326 or conductor 327 to the altering agent. Preferably, this alteration occurs by subjecting the wafer to a nitrogen gas (preferably N_2) which is incorporated in a plasma. This step preferably is performed at an ambient temperature or around 300 to 500 C for around 20 seconds to 2 minutes. The goal of this step is to substantially completely convert the Ta, Mo or Ti into Ta_xN_y, Mo_xN_y, or Ti_xN_y.

[0022] Once this alteration is accomplished and the gate structures are patterned and etched, another conductive material 328 may be formed in step 220 so as to fill the remaining portion of the gate electrode (if necessary). Preferably, this additional conductive material 328 is comprised of tungsten, aluminum or other conductive material.

[0023] Although specific embodiments of the present invention are herein described, they are not to be construed as limiting the scope of the invention. Many embodiments of the present invention will become apparent to those skilled in the art in light of methodology of the specification. The scope of the invention is limited only by the claims appended.

Claims

1. A method of forming a first transistor having a first gate electrode and a second transistor having a second gate electrode on a semiconductor substrate, said method comprising the steps of:

   forming a conductive material insulatively disposed over said semiconductor substrate, said

conductive material having a work function; and

altering a portion of the conductive material so as to change the work function of said altered conductive material, said conductive material to form said first gate electrode and said altered conductive material to form said second gate electrode.

2. The method of claim 1, wherein said first transistor is an NMOS device and said second transistor is a PMOS device.

3. The method of claim 2, wherein said first transistor and said second transistor form a CMOS device.

4. The method of claim 1, wherein said conductive material is comprised of a conductor selected from the group consisting of: Ta, Mo, Ti and any combination thereof.

5. The method of claim 1, wherein said step of altering a portion of said conductive matetial is comprised of: subjecting said portion of said conductive material to a plasma which incorporates a nitrogen-containing gas.

6. The method of claim 1, forming a conductive material comprising the steps of:

forming a first conductive material insulatively disposed over a first portion of said semiconductor substrate, said first conductive material having a first work function;

forming a second conductive material insulatively disposed over a second portion of said semiconductor substrate, said second conductive material is comprised of said first conductive material but has a second work function which is different than said first work function; and wherein said first conductive material is used to form said first gate electrode and said second conductive material is used to form said second gate electrode.

7. The method of claim 6, wherein said first conductive material is comprised of Ta and said second conductive material is comprised of Ta_xN_y.

8. The method of claim 6, wherein said first conductive material is comprised of Mo and said second conductive material is comprised of Mo_xN_y.

9. The method of claim 6, wherein said first conductive material is comprised of Ti and said second conductive material is comprised of Ti_xN_y.

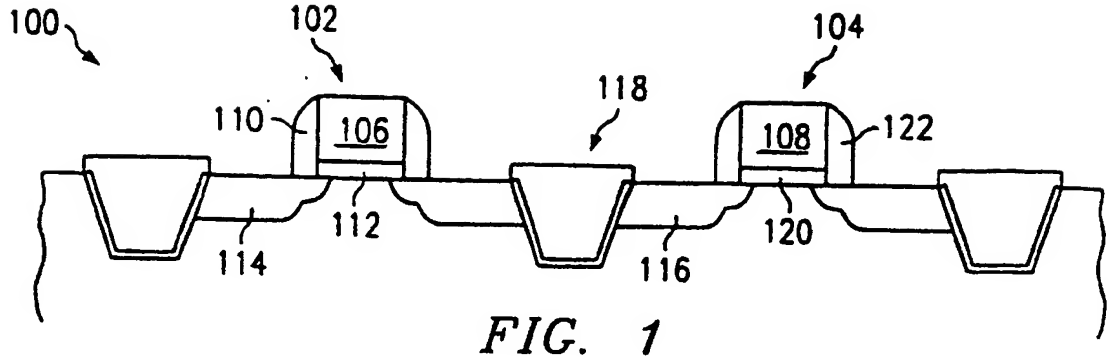

FIG. 1

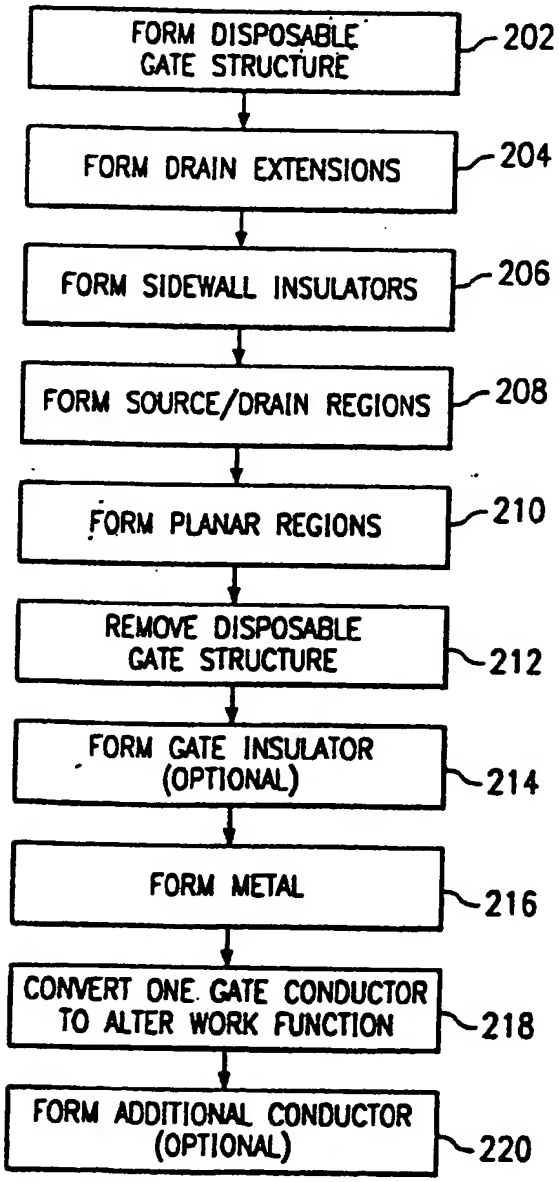

FIG. 2

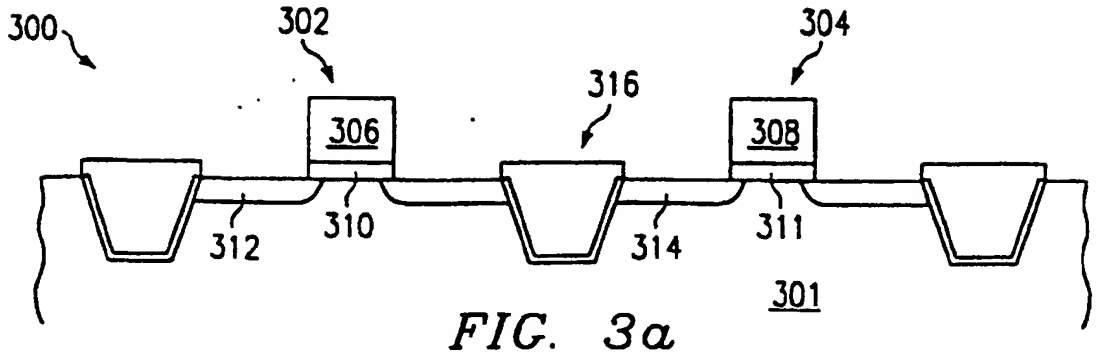

FIG. 3a

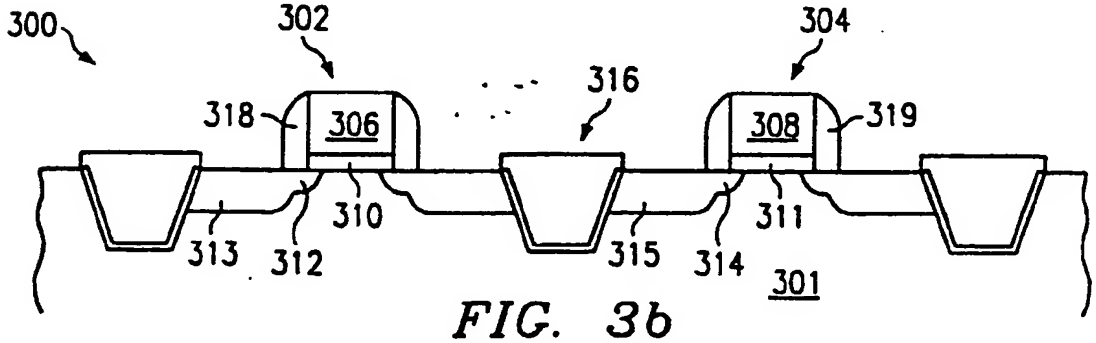

FIG. 3b

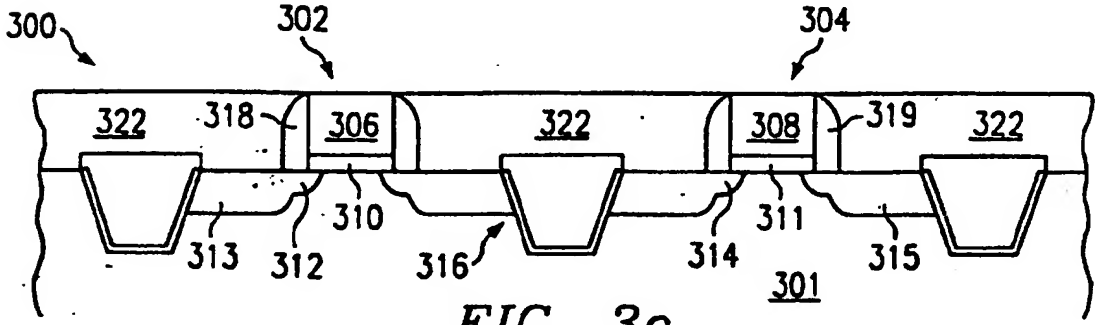

FIG. 3c

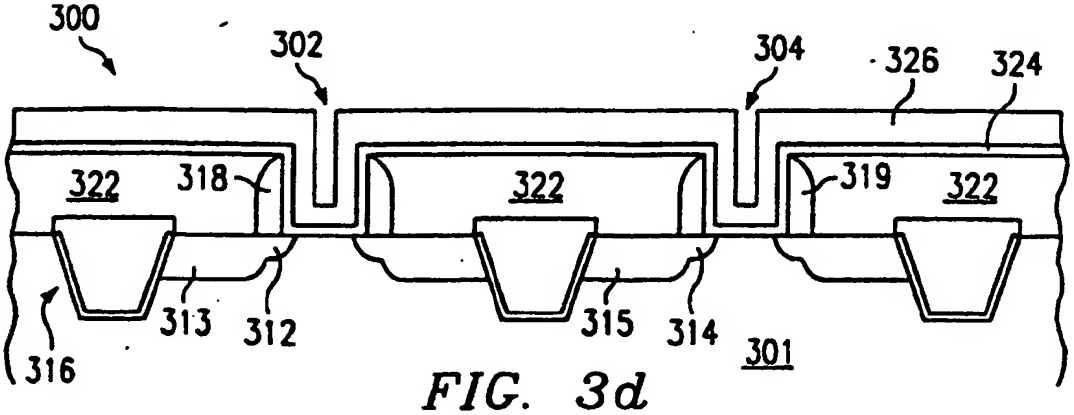

FIG. 3d

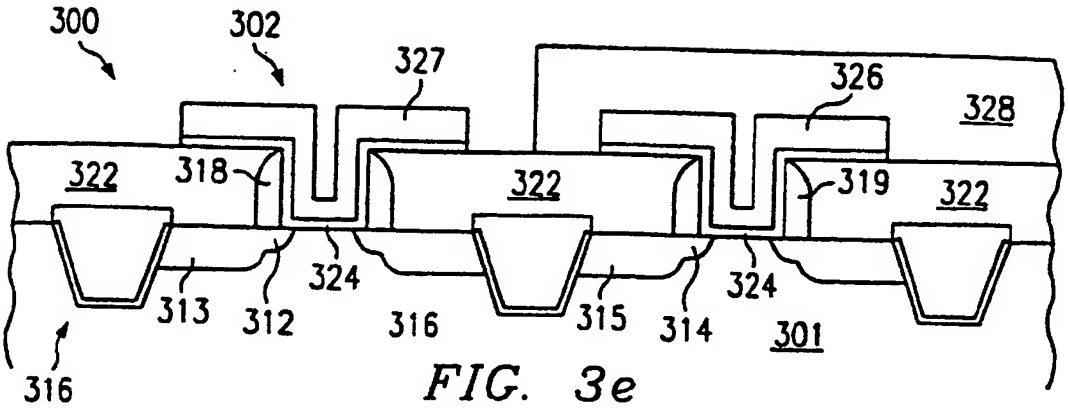

FIG. 3e

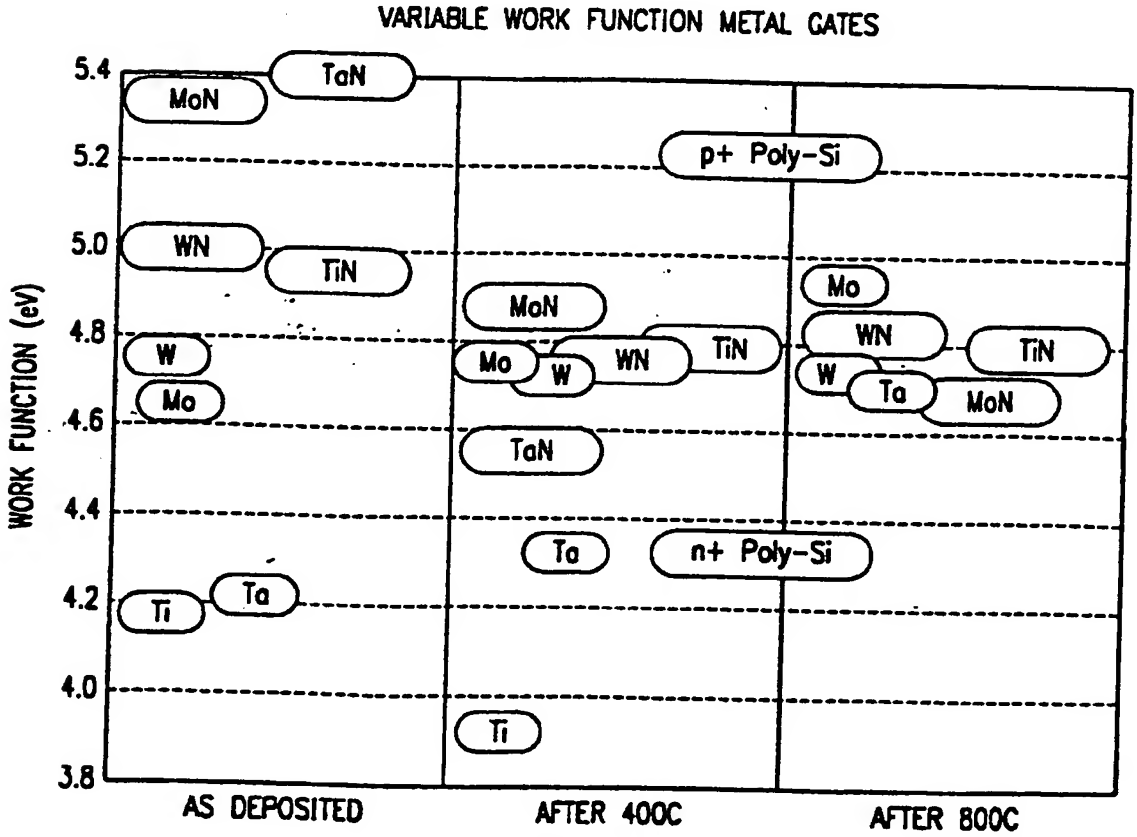

FIG. 4

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 032 033 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
12.05.2004 Bulletin 2004/20

(43) Date of publication A2:
30.08.2000 Bulletin 2000/35

(21) Application number: **00103406.5**

(22) Date of filing: **24.02.2000**

(51) Int Cl.[7]: **H01L 21/8234**, H01L 21/8238

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **26.02.1999 US 121786 P**

(71) Applicant: **Texas Instruments Incorporated**
Dallas, Texas 75251 (US)

(72) Inventors:
- **Wilks, Glen D.**
  Dallas, Texas 75243 (US)
- **Summerfelt, Scott R.**
  Cupertino, California 95014 (US)

(74) Representative:
Degwert, Hartmut, Dipl.-Phys. et al
Prinz & Partner GbR,
Manzingerweg 7
81241 München (DE)

(54) Method of forming dual metal gate structures for CMOS devices

(57) An embodiment of the instant invention is a method of forming a first transistor having a first gate electrode and a second transistor having a second gate electrode on a semiconductor substrate, the method comprising the steps of: forming a conductive material (step 216 of FIGURE 2) insulatively disposed over the semiconductor substrate, the conductive material having a work function; and altering a portion of the conductive material (step 218 of FIGURE 2) so as to change the work function of the altered conductive material, the conductive material to form the first gate electrode and the altered conductive material to form the second gate electrode. Preferably, the first transistor is an NMOS device, the second transistor is a PMOS device, and the first transistor and the second transistor form a CMOS device. The conductive material is, preferably, comprised of a conductor selected from the group consisting of: Ta, Mo, Ti and any combination thereof. Preferably, the step of altering a portion of the conductive material is comprised of: subjecting the portion of the conductive material to a plasma which incorporates a nitrogen-containing gas.

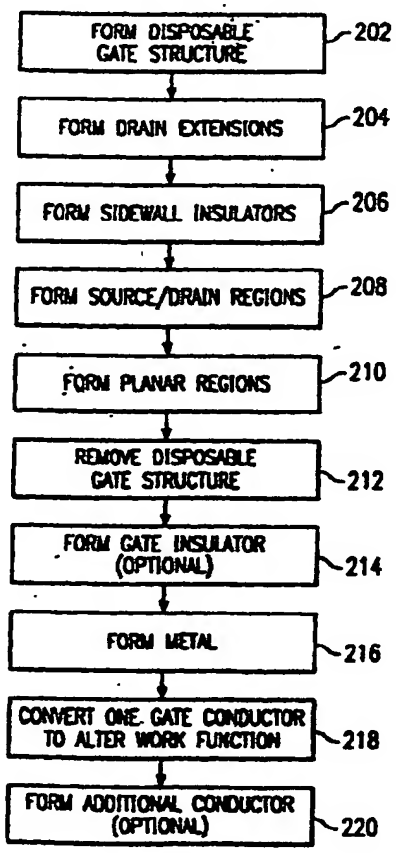

FIG. 2

EP 1 032 033 A3

Printed by Jouve, 75001 PARIS (FR)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 10 3406

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 764 982 A (SIEMENS AG) 26 March 1997 (1997-03-26) * column 1, line 3-7,28-32 * * column 9, line 15-20 * * column 10, line 9-14 *	1-3,6	H01L21/8234 H01L21/8238
Y	---	4	
Y	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 02, 26 February 1999 (1999-02-26) -& JP 10 294455 A (MOTOROLA INC), 4 November 1998 (1998-11-04)	4	
A	-& US 6 084 279 A (OLOWOLAFE J OLUFEMI ET AL) 4 July 2000 (2000-07-04) * column 3, line 7-15; figure 8 *	5	
A	--- US 5 391 510 A (MATHAD GANGADHARA S ET AL) 21 February 1995 (1995-02-21) * figures 1,2 *	1	
P,X	--- US 6 027 961 A (FRISA LARRY E ET AL) 22 February 2000 (2000-02-22) * figures 1-9 *	1-9	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 March 2004	Koskinen, T.J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 10 3406

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

19-03-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0764982 A	26-03-1997	DE 19535629 C1	12-09-1996
		DE 59608424 D1	24-01-2002
		EP 0764982 A1	26-03-1997
		JP 9129752 A	16-05-1997
		TW 398056 B	11-07-2000
		US 5882964 A	16-03-1999
JP 10294455 A	04-11-1998	US 6084279 A	04-07-2000
US 5391510 A	21-02-1995	NONE	
US 6027961 A	22-02-2000	CN 1243336 A ,B	02-02-2000
		JP 2000031296 A	28-01-2000
		TW 459351 B	11-10-2001

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82